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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,042	10/17/2003	Clifford A. Zitlaw	2960P	9207

7590 03/17/2006

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EXAMINER	
PORTKA, GARY J	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,042	ZITLAW, CLIFFORD A.	
	Examiner	Art Unit	
	Gary J. Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6 Feb 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 are presented for examination.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on February 6, 2004 was considered by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson, US 6,765,812 B2, in view of Takemae, US 6,650,593 B2.

5. As to claims 1-2, 6-9, 13-15, 18, 20, 22, 25, and 27, Anderson discloses a memory module, method, and medium for an embedded PC system (see Abstract, Fig. 1) comprising a flash device and interface coupled to a first chip select of a dedicated SDRAM bus, utilized to access the flash (see col. 3 lines 23-42, col. 7 line 54 to col. 8 line 3, Fig. 2, and col. 11 lines 48-67) wherein the flash functions substantially as a hard disk (since Applicant has admitted as prior art that such solid state devices are used to function as hard disks; alternatively, the "wherein" clause merely describes an effect of the other claim elements that is inherent to the extent recited).

6. Anderson does not disclose the flash is a NAND device. However, use of a NAND type flash in an entirely analogous system is taught by Takemae (see Figs. 2-4).

Since NAND type flash devices were known to be desirable in a system interfacing flash to a SDRAM bus (see Takemae col. 2 lines 38-48, col. 6 lines 3-10, and col. 8 lines 40-45), an artisan would have been motivated to use NAND flash in the Anderson system. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a NAND device, because NAND flash was known to be useful for interfacing to a SDRAM bus.

7. As to claims 3, 10, 19, and 26, Anderson discloses SDRAM and flash (obviously NAND as taught by Takemae) on first and second sides of a memory module (see Anderson col. 12 line 66 to col. 13 line 1).

8. As to claims 4-5, 11-12, 16-17, 21, 23-24, and 28, clearly the devices of Anderson can be adapted to be directly soldered as recited.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent No:

6,721,840 Interfacing to synchronous dynamic and static memory.

6,721,212 Controller for plurality of memories via logic interfaces.

6,266,282 Synchronous flash and RAM sharing system bus.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J Portka
Primary Examiner
Art Unit 2188

March 13, 2006

GARY PORTKA
PRIMARY EXAMINER